What is claimed is:

1. An electrode structure, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of conductive material formed on the conductive binding layer.

2. The electrode structure of claim 1, wherein the binding layer is at least semiconductive and is formed from an oxide layer by annealing the electrode structure to cause conductive material from the second layer to be chemisorbed into the oxide layer.

3. The electrode structure of claim 2, wherein the electrode structure is annealed at a selected temperature for a predetermined period of time to control the chemisorption of conductive material from the second layer into the oxide layer.

4. The electrode structure of claim 1, wherein the first layer is a metal that adheres to an oxide.

5. The electrode structure of claim 1, wherein the second layer is a metal that is diffusible into an oxide and bonds to an oxide.

6. An electrode structure, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer including a silicon dioxide formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of conductive material formed on the binding layer, wherein the conductive material of the second layer is selected to be diffusible into the binding layer to make the binding layer capable of conducting electrical current.

7. An electrode structure, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of conductive material formed on the conductive binding layer, wherein the binding layer is selected to provide adhesion between the first and second layers to prevent the second layer from being forced out of the opening in the dielectric layer by forces created by a chemical/mechanical planarization process being applied to the electrode structure.

8. An electrode structure, comprising:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of metallization formed on the binding layer.

9. The electrode structure of claim 8, wherein the first layer of metallization is one of tungsten and nickel.

10. The electrode structure of claim 8, wherein the second layer of metallization is one of silver and nickel.

11. The electrode structure of claim 8, wherein the binding layer is at least semiconductive and is formed from an oxide layer by annealing the electrode structure to cause metal from the second layer to diffuse into the oxide layer.

12. An electrode structure, comprising:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of metallization formed on the binding layer, wherein the binding layer is selected to provide adhesion between the first and second layers of metallization to prevent the second layer of metallization from being forced out of the opening in the dielectric layer by forces created by a chemical/mechanical planarization process being applied to the electrode structure to form an isolated metallization structure in the opening in the dielectric layer.

13. The electrode structure of claim 12, wherein the binding layer includes an oxide and a metal diffused from the second layer into the oxide.

14. An electrode structure, comprising:

a first layer of one of tungsten, nickel and semiconductor material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of silver formed on the binding layer, wherein the conductive binding layer includes an oxide and silver diffused from the second layer into the oxide.

15. An electrode structure, comprising:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of metallization formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and metal diffused from the second layer by annealing the electrode structure at a selected temperature for a predetermined period of time.

16. The electrode structure of claim 15, wherein the second layer of metallization is silver and wherein the conductive binding layer includes an oxide and silver diffused from the second layer into the oxide to provide adhesion between the first layer and the second layer during planarization to form a damascene silver layer in the opening.

17. The electrode structure of claim 16, wherein the silver is diffused into the TEOS by annealing the electrode structure at a temperature of about 350° Celsius for about ten minutes.

18. An electrode structure, comprising:

a first layer of conductive material;

a first dielectric layer formed on a surface of the first layer;

a second dielectric layer formed on the first dielectric layer, wherein the first dielectric layer has a faster etch rate than the second dielectric layer;

an opening formed in the first and second dielectric layers to expose a portion of the surface of the first layer, wherein the opening has a reentrant profile in response to the difference in etch rate between the first and second dielectric layers;

a binding layer formed on the first dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of conductive material formed on the conductive binding layer.

19. A memory cell, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

20. The memory cell of claim 19, wherein the layer of chalcogenide material is doped by diffusing conductive material from the third layer into the chalcogenide layer.

21. The memory cell of claim 20, wherein the third layer comprises one of silver, nickel and polysilicon.

22. A memory cell, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of germanium selenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped germanium selenide material.

23. The memory cell of claim 22, wherein the concentration ratio of germanium to selenide in the layer of germanium selenide is between about 15/85 and about 40/60.

24. A memory cell, comprising:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer including one of silver or nickel formed on the layer of chalcogenide material, wherein the layer of chalcogenide material is doped by annealing to cause some of the silver or nickel from the third layer to diffuse into the chalcogenide layer.

25. The memory cell of claim 24, wherein the layer of chalcogenide material is germanium selenide.

26. A memory cell, comprising:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of metalization formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and metal diffused from the second layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

27. The memory cell of claim 26, wherein the second layer of metalization is one of silver or nickel and wherein the conductive binding layer includes an oxide and silver or nickel diffused into the oxide from the second layer by annealing at a selected temperature for a predetermined period of time.

28. The memory cell of claim 26, wherein the layer of chalcogenite material is doped by diffusing conductive material from the third layer into the layer of chalcogenide material.

29. A memory cell, comprising:

a first layer of one of tungsten, nickel or polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of one of silver or nickel formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and silver or nickel diffused into the silicon dioxide from the second layer to form the conductive layer by annealing at a selected temperature for a predetermined period of time;

a layer of germanium selenide material formed on the second layer of silver or nickel; and

a third layer including silver or nickel formed on the layer of germanium selenide, wherein the layer of germanium selenide material is doped by ultra violet annealing for a selected time period to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

30. A memory cell, comprising:

a first layer of conductive material;

a first dielectric layer formed on a surface of the first layer;

a second dielectric layer formed on the first dielectric layer;

an opening formed in the first and second dielectric layers to expose a portion of the surface of the first layer, wherein the opening includes a reentrant

profile in response to a difference in an etch rate between the first and second dielectric layers;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of chalcogenide, wherein the layer of chalcogenide material is doped by diffusing conductive material from the third layer into the layer of chalcogenide.

31. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of chalcogenide material, wherein the memory cell is annealed to cause conductive material from the third layer to diffuse into the layer of chalcogenide material to dope the layer of chalcogenide material.

32. The memory system of claim 31, wherein the binding layer is at least semiconductive and is formed from an oxide layer by annealing to cause conductive material from the second layer to be chemisorbed into the oxide layer.

33. The memory system of claim 31, wherein the binding layer is selected to provide adhesion between the first and second layers.

34. The memory system of claim 31, wherein the second layer is a metal that is diffusible into an oxide and bonds to an oxide.

35. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of germanium selenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of germanium selenide, wherein the layer of germanium selenide is doped by ultra violet annealing to cause conductive material from the third layer to diffuse into the layer of germanium selenide.

36. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of metallization formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and metal diffused from the second layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

37. A memory system, comprising:

an array of memory elements, each memory element including:

a first layer of one of tungsten, nickel or polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of one of silver or nickel formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and silver or nickel diffused into the silicon dioxide from the second layer to form the conductive binding layer by annealing at a selected temperature for a predetermined period of time;

a layer of germanium selenide material formed on the second layer of silver or nickel; and

a third layer including silver or nickel formed on the layer of germanium selenide, wherein the layer of germanium selenide material is doped by ultra violet annealing for a selected time period to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

38. A memory system, comprising:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a programmable memory cell coupled to another source/drain terminal of the transistor, wherein the programmable memory cell includes:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

39. A memory system, comprising:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a programmable memory cell coupled to another source/drain terminal of the transistor, wherein the programmable memory cell includes:

a first layer of one of metallization or polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of one of silver or nickel formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and silver or nickel diffused into the silicon dioxide from the second layer to form the conductive binding layer by annealing at a selected temperature for a predetermined period of time;

a layer of germanium selenide material formed on the second layer of silver or nickel; and

a third layer including silver or nickel formed on the layer of germanium selenide, wherein the layer of germanium selenide material is doped by ultra violet annealing for a selected time period to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

40. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit includes at least one electrode, the at least one electrode including:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of conductive material formed on the conductive binding layer.

41. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one electrode structure, the at least one electrode structure including:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of metallization formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and metal diffused from the second layer by annealing the electrode structure at a selected temperature for a predetermined period of time.

42. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises at least one electrode structure, the at least one electrode structure including:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of metallization formed on the binding layer, wherein the binding layer is selected to provide adhesion between the first and second layers of metallization to prevent the second layer of metallization from being forced out of the opening in the dielectric layer by forces created by a chemical/mechanical planarization process being applied to the electrode structure to form an isolated metallization structure formed in the opening in the dielectric layer.

43. A semiconductor die, comprising:

a substrate; and

an integrated circuit formed on the substrate, wherein the integrated circuit comprises at least one electrode structure, including:

a first layer of one of tungsten, nickel and polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer; and

a second layer of silver formed on the binding layer, wherein the conductive binding layer includes a silicon dioxide and silver diffused from the second layer into the silicon dioxide to provide adhesion between the first layer and the second layer during planarization to form a damascene silver layer in the opening.

44. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

45. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising at least one memory element including:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of germanium selenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of germanium selenide, wherein the layer of germanium selenide is doped by ultra violet annealing to cause conductive material from the third layer to diffuse into the layer of germanium selenide.

46. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including:

a first layer of metallization;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of metalization formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and metal diffused from the second layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

47. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system comprising an array of memory elements and each memory element including:

a first layer of one of tungsten, nickel or polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of one of silver or nickel formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and silver or nickel diffused into the silicon dioxide from the second layer to form the conductive binding layer by annealing at a selected temperature for a predetermined period of time;

a layer of germanium selenide material formed on the second layer of silver or nickel; and

a third layer including silver or nickel formed on the layer of germanium selenide, wherein the layer of germanium selenide material is doped by ultra violet annealing for a selected time period to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

48. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system including:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a programmable memory cell coupled to another source/drain terminal of the transistor, wherein the programmable memory cell includes:

a first layer of conductive material;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of conductive material formed on the binding layer;

a layer of doped chalcogenide material formed on the second layer of conductive material; and

a third layer of conductive material formed on the layer of doped chalcogenide material.

49. An electronic system, comprising:

a processor; and

a memory system coupled to the processor, the memory system including:

an array of memory elements arranged in rows and columns;

a plurality of address lines each coupled to one of a row or a column of memory elements; and

a plurality of data lines each coupled to one of a row or a column of memory elements, each memory element including:

a transistor including a gate terminal coupled to an address line and a source/drain terminal coupled to a data line; and

a programmable memory cell coupled to another source/drain terminal of the transistor, wherein the programmable memory cell includes:

a first layer of one of metallization or polysilicon;

a dielectric layer formed on a surface of the first layer;

an opening formed in the dielectric layer to expose a portion of the surface of the first layer;

a conductive binding layer formed on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer of one of silver or nickel formed on the conductive binding layer, wherein the conductive binding layer includes a silicon dioxide and silver or nickel diffused into the silicon dioxide from the second layer to form the conductive binding layer by annealing at a selected temperature for a predetermined period of time;

a layer of germanium selenide material formed on the second layer of silver or nickel; and

a third layer including silver or nickel formed on the layer of germanium selenide, wherein the layer of germanium selenide material is doped by ultra violet annealing for a selected time period to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

50. A method of making an electrode structure, comprising:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer; and

forming a second layer of conductive material on the binding layer.

51. The method of claim 50, wherein forming the binding layer comprises:

forming an oxide layer; and

annealing the electrode structure to cause conductive material from the second layer to be chemisorbed into the oxide layer.

52. The method of claim 51, further comprising controlling the chemisorption of conductive material from the second layer into the oxide layer by annealing at a selected temperature for a predetermined time period.

53. The method of claim 50, further comprising selecting a metal that is diffusible into an oxide for the second layer of material.

54. The method of claim 50, further comprising planarizing the electrode structure by a chemical/mechanical planarization process.

55. A method of making a electrode structure, comprising:

forming a first layer of metallization;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of metallization on the binding layer;

annealing the electrode structure to cause metallization from the second layer to diffuse into the binding layer and to provide adhesion between the first and second layers of metallization; and

planarizing the electrode structure by a chemical/mechanical planarization process to form an isolated metallization structure formed in the opening in the dielectric layer.

56. A method of making an electrode structure, comprising:

forming a first layer including one of tungsten, nickel and polysilicon;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including a silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer including one of silver and nickel on the binding layer;

annealing the electrode structure at a selected temperature for a predetermined time period to control the chemisorption of silver or nickel into the binding layer; and

planarizing the electrode structure to form a damascene silver layer in the opening.

57. A method of making an electrode structure, comprising:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening including a reentrant profile in the dielectric layer to expose a portion of the surface of the first layer;

forming a conductive binding layer on the dielectric layer and on the exposed portion of the surface of the first layer; and

forming a second layer of conductive material on the conductive binding layer.

58. A method of making an electrode structure, comprising:

forming a first layer including one of tungsten, nickel and polysilicon;

forming a first dielectric layer on a surface of the first layer;

forming a second dielectric layer on the first dielectric layer, wherein the first dielectric layer has an etch rate faster than the second dielectric layer;

forming an opening in the first and second dielectric layers to expose a portion of the surface of the first layer, wherein the opening includes a reentrant profile in response to a difference in the etch rate between the first and second dielectric layers;

forming a binding layer including a silicon dioxide on the second dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer including one of silver and nickel on the binding layer;

annealing the electrode structure at a selected temperature for a predetermined time period to control the chemisorption of silver or nickel into the binding layer; and

planarizing the electrode structure to form a damascene silver layer in the opening.

59. A method of making a memory cell, comprising:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

60. A method of making a memory cell, comprising:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of germanium selenide material on the second layer of conductive material;

forming a third layer of conductive material on the layer of germanium selenide; and

annealing the memory cell to cause conductive material from the third layer to diffuse into the layer of germanium selenide.

61. The method of claim 60, wherein the concentration of germanium to selenide in the germanium selenide layer is between about 15/85 and about 40/60.

62. A method of making a memory cell, comprising:

forming a first layer of metallization;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of metallization on the binding layer;

diffusing metallization from the second layer into the binding layer;

forming a layer of chalcogenide material on the second layer of metallization;

forming a third layer of metallization on the layer of chalcogenide material; and

annealing the memory cell to cause metallization from the third layer to diffuse into the layer of chalcogenide material.

63. A method of making a memory cell, comprising:

forming a first layer of one of tungsten, nickel or polysilicon;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including a silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of one of silver or nickel on the conductive binding layer;

diffusing silver or nickel into the binding layer from the second layer by annealing at a selected temperature for a predetermined period of time;

forming a layer of germanium selenide material on the second layer of silver or nickel;

forming a third layer including silver or nickel on the layer of germanium selenide; and

annealing the memory cell to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

64. A method of making a memory cell, comprising:

forming a first layer of conductive material;

forming a first dielectric layer on a surface of the first layer;

forming a second dielectric layer on the first dielectric layer;

forming an opening in the first and second dielectric layers to expose a portion of the surface of the first layer, wherein the opening includes a reentrant profile in response to a difference in an etch rate between the first and second dielectric layers;

forming a binding layer on the second dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of chalcogenide material on the second layer of conductive material;

forming a third layer of conductive material on the layer of chalcogenide material; and

annealing the memory cell to cause conductive material from the third layer to be chemisorbed by the layer of chalcogenide material.

65. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

66. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of germanium selenide material on the second layer of conductive material;

forming a third layer of conductive material on the layer of germanium selenide material; and

annealing the memory cell to cause conductive material from the third layer to diffuse into the layer of germanium selenide.

67. A method of making a memory system, comprising:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of one of tungsten, nickel or polysilicon;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including a silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of one of silver or nickel on the conductive binding layer;

diffusing silver or nickel into the binding layer from the second layer by annealing at a selected temperature for a predetermined period of time;

forming a layer of germanium selenide material on the second layer of silver or nickel;

forming a third layer including silver or nickel on the layer of germanium selenide; and

annealing the memory cell to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

68. A method of making a memory system, comprising:

forming an array of memory elements arranged in rows and columns;

forming a plurality of address lines each coupled to one of a row or a column of memory elements; and

forming a plurality of data lines each coupled to one of a row or a column of memory elements, wherein forming each memory element includes:

forming a transistor including a gate terminal coupled to one of the plurality of address lines and a source/drain terminal coupled to one of the plurality of data lines; and

forming a memory cell coupled to another source/drain terminal of the transistor, wherein forming the memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

69. A method of making a memory system, comprising:

forming an array of memory elements arranged in rows and columns;

forming a plurality of address lines each coupled to one of a row or a column of memory elements; and

forming a plurality of data lines each coupled to one of a row or a column of memory elements, wherein forming each memory element includes:

forming a transistor including a gate terminal coupled to one of the plurality of address lines and a source/drain terminal coupled to one of the plurality of data lines; and

forming a memory cell coupled to another source/drain terminal of the transistor, wherein forming the memory cell includes:

forming a first layer of one of tungsten, nickel or polysilicon;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including a silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of one of silver or nickel on the conductive binding layer;

diffusing silver or nickel into the binding layer from the second layer by annealing at a selected temperature for a predetermined period of time;

forming a layer of germanium selenide material on the second layer of silver or nickel;

forming a third layer including silver or nickel on the layer of germanium selenide; and

annealing the memory cell to cause a predetermined level of chemisorption of silver or nickel from the third layer to diffuse into the layer of germanium selenide material.

70. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming an electrode coupled to the integrated circuit, wherein forming the electrode includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer; and

forming a second layer of conductive material on the conductive binding layer.

71. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming an electrode structure associated with the integrated circuit, wherein forming the electrode structure includes:

forming a first layer of metallization;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of metallization on the binding layer;

annealing the electrode structure to cause metallization from the second layer to diffuse into the binding layer and to provide adhesion between the first and second layers of metallization; and

planarizing the electrode structure by a chemical/mechanical planarization process to form an isolated metallization structure formed in the opening in the dielectric layer.

72. A method of making a semiconductor die, comprising:

providing a substrate;

forming an integrated circuit supported by the substrate; and

forming an electrode structure associated with the integrated circuit, wherein forming the electrode structure includes:

forming a first layer including one of tungsten, nickel and polysilicon;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer including a silicon dioxide on the dielectric layer and on the exposed portion of the surface of the first layer;

a second layer including one of silver and nickel on the binding layer;

annealing the electrode structure at a selected temperature for a predetermined time period to control the chemisorption of silver or nickel into the binding layer; and

planarizing the electrode structure to form a damascene silver layer in the opening.

73. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor, wherein forming the memory system includes:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

74. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor, wherein forming the memory system includes:

forming an array of memory elements; and

forming a memory cell associated with each memory element, wherein forming each memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of germanium selenide material on the second layer of conductive material;

forming a third layer of conductive material on the layer of conductive material; and

annealing the memory cell to cause conductive material from the third layer to diffuse into the layer of germanium selenide.

75. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor and including a plurality of memory cells, wherein forming the memory system:

forming an array of memory elements arranged in rows and columns;

forming a plurality of address lines each coupled to one of a row or a column of memory elements; and

forming a plurality of data lines each coupled to one of a row or a column of memory elements, wherein forming each memory element includes:

forming a transistor including a gate terminal coupled to one of the plurality of address lines and a source/drain terminal coupled to one of the plurality of data lines; and

forming a memory cell coupled to another source/drain terminal of the transistor, wherein forming the memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the layer of doped chalcogenide material.

76. A method of making an electronic system, comprising:

forming a processor; and

forming a memory system coupled to the processor and including a plurality of memory cells, wherein forming the memory system:

forming an array of memory elements arranged in rows and columns;

forming a plurality of address lines each coupled to one of a row or a column of memory elements; and

forming a plurality of data lines each coupled to one of a row or a column of memory elements, wherein forming each memory element includes:

forming a transistor including a gate terminal coupled to one of the plurality of address lines and a source/drain terminal coupled to one of the plurality of data lines; and

forming a memory cell coupled to another source/drain terminal of the transistor, wherein forming the memory cell includes:

forming a first layer of conductive material;

forming a dielectric layer on a surface of the first layer;

forming an opening in the dielectric layer to expose a portion of the surface of the first layer;

forming a binding layer on the dielectric layer and on the exposed portion of the surface of the first layer;

forming a second layer of conductive material on the binding layer;

forming a layer of doped chalcogenide material on the second layer of conductive material; and

forming a third layer of conductive material on the doped layer of chalcogenide material.